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By: 7/2/

Attorney Docket No.: 16869N-039000US Client Reference No.: NT0490US

8/IDS. 1.57eptel 5-9-02

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Keizo Takechi, et al.

Application No.:

Filed: Herewith

For: Driver Circuit Integrated with Load Current Output Circuit, Pin Electronics and IC Tester Having

Thereof

Examiner:

Unassigned

Art Unit:

Unassigned

INFORMATION DISCLOSURE STATEMENT

UNDER 37 CFR §1.97 and §1.98

Assistant Commissioner for Patents Washington, D.C. 20231

Sir:

The references cited on attached form PTO/SB/08A are being called to the attention of the Examiner. Copies of the references are enclosed. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

Applicant believes that <u>no fee is required</u> for submission of this statement, since it is being submitted prior to the first Office Action. However, if a fee is required, the

Keizo Takechi, et al. Application No.: Page +

Commissioner is authorized to deduct such fee from Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,

James M. Heslin Reg. No. 29,541

TOWNSEND and TOWNSEND and CREW LLP Two Embarcadero Center, 8<sup>th</sup> Floor San Francisco, California 94111-3834 Tel: 650-326-2400

Fax: 650-326-2422 JMH/RCC:mks

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